I Claim:

1. A configurable despreader for processing digital data, the despreader comprising:

a plurality of data lines for receiving a plurality of input data types;

at least one selective coupler coupled to the plurality of data lines;

a first multiplier coupled to the selective coupler, the first multiplier for multiplying a desired input data type received from the selective coupler with a despreading code chip to produce a first observation; and

a first code input line coupled to the multiplier, the first code input line for receiving a despreading code chip;

wherein the selective coupler selectively couples one of the plurality of data lines with the multiplier per any one of a plurality of despreading protocols.

2. The despreader recited in Claim 1 wherein the plurality of data lines comprise:

an in-phase sample (I-sample) line for receiving an in-phase data sample;

a quadrature-phase sample (Q-sample) line for receiving a quadrature-phase data sample; and

a quadrature-phase code (Q-code) line for receiving a quadrature-phase code chip;

wherein the selective coupler is coupled to the I-sample line, the Q-sample line and the multiplier, wherein the Q-code line is also coupled to the first multiplier, and wherein the selective coupler selectively couples either the I-sample line or the Q-sample line to the first multiplier.

3. The despreader recited in Claim 2 further comprising:

a first accumulate and dump circuit coupled to the first multiplier, the first accumulate and dump circuit receiving the first observation from the first multiplier and having an enable input that selectively dumps a first accumulated sample after an observation period has been satisfied.

4. The despreader recited in Claim 3 further comprising:

a second multiplier coupled to an additional code input line and to one of the plurality of data lines per a common portion of the plurality of despreading protocols.

5. The despreader recited in Claim 4 further comprising:

an in-phase code (I-code) input line for receiving an in-phase code chip;

wherein the second multiplier is coupled to the I-code input line and to the I-sample input line, the second multiplier for multiplying an I-code input and an I-sample input to produce a second observation.

6. The despreader recited in Claim 5 further comprising:

a second accumulate and dump circuit coupled to the second multiplier, the second accumulate and dump circuit receiving the second observation output by the second multiplier and having an enable input that selectively dumps a second accumulated sample after the observation period has been satisfied.

7. The despreader recited in Claim 6 further comprising:

an interface circuit coupled to the first accumulate and dump circuit and the second accumulate and dump circuit, the interface circuit having an enable input allowing the interface circuit to communicate a detection statistic.

8. The despreader recited in Claim 1 further comprising:

a memory coupled to the selective coupler, the memory storing a value that enables the selective coupler to communicate a desired input data sample.

9. The despreader recited in Claim 7 further comprising:

a memory coupled to the first accumulate and dump circuit and the second accumulate and dump circuit, the memory storing a value that dictates the observation period for the first accumulate and dump circuit and the second accumulate and dump circuit.

10. The despreader recited in Claim 7 further comprising:

an additional selective coupler coupled to the I-sample line and the Q-sample line; and

a third multiplier coupled to the additional selective coupler and the I-code line;

wherein the additional selective coupler is coupled to the I-sample line, the Q-sample line and the third multiplier, wherein the I-code line is also coupled to the multiplier, and wherein the selective coupler selectively couples either the I-sample line or the Q-sample line to the third multiplier per any one of multiple despreading protocols.

11. The despreader recited in Claim 10 further comprising:

a third accumulate and dump circuit coupled to the third multiplier, the third accumulate and dump circuit receiving a third observation output by the third multiplier and having an enable input that selectively dumps an accumulated sample after the observation period has been satisfied.

12. The despreader recited in Claim 11 further comprising:

a fourth multiplier coupled to the Q-code input line and to the Q-sample input line, the fourth multiplier for multiplying the Q-code input and the Q-sample input to produce a fourth observation.

13. The despreader recited in Claim 12 further comprising:

a fourth accumulate and dump circuit coupled to the fourth multiplier, the fourth accumulate and dump circuit receiving the fourth observation output by the fourth multiplier and having an enable input that selectively dumps an accumulated sample after the observation period has been satisfied.

14. The despreader recited in Claim 13 further comprising:

an additional interface circuit coupled to the third accumulate and dump circuit and to the fourth accumulate and dump circuit, the additional interface circuit having an enable input allowing the additional interface to communicate a detection statistic.

15. A despreader for processing digital data, the despreader comprising:

at least one multiplier for multiplying an input data sample with a despreading code chip; and

at least one accumulate and dump circuit coupled to the multiplier;

wherein the accumulate and dump circuit has an enable input that selectively dumps an accumulated sample after an observation period has been satisfied.

16. The despreader recited in Claim 15 wherein the accumulate and dump circuit includes a comparator coupled to the enable input, the comparator for comparing a desired observation period with the actual observation period.

17. The despreader recited in Claim 16 further comprising:

a memory coupled to the comparator, the memory for storing a value of the desired observation period.

18. The despreader recited in Claim 16 further comprising:

a counter coupled to the comparator, the counter for counting the actual observation period.

19. The despreader recited in Claim 15 further comprising:

an additional accumulate and dump circuit; and

an additional multiplier coupled to the additional accumulate and dump circuit, the additional accumulate and dump circuit receiving an output from the additional multiplier and having an enable input that selectively dumps an additional accumulated sample after the observation period has been satisfied.

20. The despreader recited in Claim 19 further comprising:

an interface circuit coupled to the accumulate and dump circuit and to the additional accumulate and dump circuit, the interface circuit having an enable input allowing the interface circuit to communicate a detection statistic.

21. The despreader recited in Claim 20 further comprising:

a memory coupled to the accumulate and dump circuit and the additional accumulate and dump circuit, the memory storing a value that dictates the observation length.

22. The despreader recited in Claim 20 wherein the observation length is determined by a noise level of a signal being despread.

23. A configurable electronic communication device for processing data, the electronic communication device comprising:

a radio frequency/intermediate frequency (RF/IF) transceiver;

an analog to digital (A/D) converter coupled to the RF/IF transceiver; and

a despreader having at least one multiplier coupled to a code input line and selectively coupled to a plurality of data input lines in a manner to satisfy any one of multiple despreading protocols.

24. The electronic communication device recited in Claim 23 wherein the despreader includes at least one selective coupler coupled to the multiplier and the plurality of data input lines, the selective coupler for selectively choosing one of the plurality of data input lines to be coupled to the multiplier for a despreading operation.

25. The electronic communication device recited in Claim 24 further comprising:

a memory coupled to the selective coupler, the memory providing a signal that enables one of the plurality of data input lines to be coupled to the multiplier for the despreading operation.

26. The electronic communication device recited in Claim 23 wherein the data processed is for a spread spectrum digital wireless protocol.

27. The electronic communication device recited in Claim 23 wherein the despreader includes at least one accumulate and dump circuit coupled to the multiplier, wherein the accumulate and dump circuit has an enable input that selectively dumps an accumulated result after an observation period has been satisfied.

28. The electronic communication device recited in Claim 27 further comprising:

an additional accumulate and dump circuit; and

an additional multiplier coupled to the additional accumulate and dump circuit, the additional accumulate and dump circuit receiving an additional observation output from the additional multiplier and having an enable input that selectively dumps an accumulated result after the observation period has been satisfied.

29. The electronic communication device recited in Claim 28 further comprising:

an interface circuit coupled to the accumulate and dump circuit and to the additional accumulate and dump circuit, the interface circuit having an enable input that allowing the interface circuit to communicate a detection statistic.

30. The electronic communication device recited in Claim 29 further comprising:

a memory coupled to the accumulate and dump circuit and the additional accumulate and dump circuit, the memory storing a value that dictates the observation period for the accumulate and dump circuit and the additional accumulate and dump circuit.

31. The electronic communication device recited in Claim 30 wherein the observation length is determined according to a noise level of a signal being despread.

32. An electronic communication device for processing data, the electronic communication device comprising:

a radio frequency (RF) transceiver;

an analog to digital (A/D) converter coupled to the RF transceiver; and

a despreader having at least one accumulate and dump circuit, the accumulate and dump circuit having an input that selectively dumps an accumulated sample after an observation period has been satisfied.

33. The electronic communication device recited in Claim 32 wherein the despreader includes a comparator coupled to the accumulate and dump circuit, the comparator for comparing a desired observation length with an actual observation length.

34. The electronic communication device recited in Claim 32 wherein the despreader includes a counter coupled to the comparator, the counter for counting the actual observation length.

35. The electronic device recited in Claim 32 further comprising:

an additional accumulate and dump circuit; and

an additional multiplier coupled to the additional accumulate and dump circuit, the additional accumulate and dump circuit receiving an additional observation from the additional multiplier and having an enable input that selectively dumps an additional accumulated sample after the observation period has been satisfied.

36. The electronic device recited in Claim 35 further comprising:

an interface circuit coupled to the accumulate and dump circuit and to the additional accumulate and dump circuit, the interface circuit having an enable input allowing the interface circuit to communicate a detection statistic.

37. The electronic device recited in Claim 36 further comprising:

a memory coupled to the accumulate and dump circuit and the additional accumulate and dump circuit, the memory storing a value that dictates the observation period for the accumulate and dump circuit and the additional accumulate and dump circuit.

38. The electronic device recited in Claim 37 wherein the observation length is determined according to a noise level of a signal being despread.

39. A method of implementing one of multiple possible despreading protocols in a configurable despreader, the method comprising:

a) receiving a plurality of input data types at a selective coupler;

b) receiving a despreading code at a multiplier;

c) selectively communicating a desired input data type to the multiplier via the selective coupler, the desired input data type selected from the plurality of input data types per a desired despreading protocol; and

d) multiplying the desired input data type with the despreading code, via the multiplier, to produce an observation.

40. The method recited in Claim 39 further comprising the steps of:

e) receiving an in-phase data sample (I-sample) at the selective coupler;

f) receiving a quadrature-phase data sample (Q-sample) at the selective coupler;

g) receiving a quadrature-phase code chip (Q-code) at the multiplier; and

h) selectively communicating either the I-sample or the Q-sample to the multiplier via the selective coupler per the desired despreading protocol.

41. The method recited in Claim 40 further comprising the step of:

i) accumulating, at an accumulate and dump circuit, the observation produced by the multiplier;

j) receiving a first control signal at the accumulate and dump circuit indicating a desired observation length;

k) repeating steps a) through j) to generate an additional observation; and

l) dumping an accumulated sample from the accumulate and dump circuit after the desired observation length has been satisfied.

42. The method recited in Claim 41 further comprising the steps of:

m) receiving an additional code chip at an additional multiplier;

n) receiving a first input data type amongst the plurality of input data types at the additional multiplier, the first input data type common between the plurality of despreading protocols; and

o) multiplying the additional code chip times the first input data type, via the additional multiplier, to produce an additional observation.

43. The method recited in Claim 41 further comprising the steps of:

m) receiving an in-phase code chip (I-code) at an additional multiplier;

n) receiving the in-phase data sample (I-sample) at the additional multiplier; and

o) multiplying the I-code with the I-sample, via the additional multiplier, to produce an additional observation.

44. The method recited in Claim 43 further comprising the steps of:

p) repeating in parallel, steps i) through k) for the additional observation at an additional accumulate and dump circuit to dump an additional accumulated sample.

45. The method recited in Claim 44 further comprising the steps of:

q) receiving the accumulated sample from the accumulate and dump circuit at an interface circuit;

r) receiving the additional accumulated sample from the additional accumulate and dump circuit at the interface circuit;

s) receiving a second control signal at the interface circuit that enables the accumulated sample and the additional accumulated sample to be transmitted as a symbol; and

t) repeating steps q) through s) for a new symbol.

46. The method recited in Claim 45 further comprising the steps of:

u) repeating in parallel steps a) through w) on a parallel set of components wherein step g) receives the in-phase code chip (I-code) at the multiplier, wherein step m) receives the quadrature-phase code chip (Q-code) at the additional multiplier, and wherein step n) receives the quadrature-phase data sample (Q-sample) at the additional multiplier.

47. A method of configurably despreading a spread spectrum signal, the method comprising:

a) receiving a first observation from a first multiplier at a despreader;

b) accumulating the first observation at a first accumulate and dump circuit;

c) receiving a first control signal at the first accumulate and dump circuit that indicates a desired observation length;

d) repeating steps a) through c) for a new observation; and

e) dumping a first accumulated sample from the first accumulate and dump circuit after the desired observation length has been satisfied.

48. The method recited in Claim 47 further comprising the steps of:

f) repeating in parallel, steps a) through e) for a second observation received from a second multiplier at a second accumulate and dump circuit, the second accumulate and dump circuit providing a second accumulated result.

49. The method recited in Claim 48 further comprising the steps of:

g) receiving the first accumulated result from the first accumulate and dump circuit at an interface circuit;

h) receiving the second accumulated result from the second accumulate and dump circuit at the interface circuit;

i) adding the first accumulated result and the second accumulated result in the interface circuit to obtain a sum;

j) receiving a second control signal at the interface circuit that enables the accumulated sample and the additional accumulated sample to be transmitted as a symbol; and

k) repeating steps g) through j) for a new symbol.

50. The method recited in Claim 49 further comprising the steps of:

n) repeating in parallel steps a) through k) on a parallel set of components for a different code chip sequence.

51. The method recited in Claim 39 wherein the desired observation length is proportional to one of a plurality of spreading factors.

52. The method recited in Claim 39 wherein the input data types can include any one of a plurality of data modulation schemes.

53. The method recited in Claim 39 wherein the despreading code can include any one of a plurality of code modulation schemes.

54. The despreader recited in Claim 1 wherein the desired observation length is proportional to one of a plurality of spreading factors.

55. The despreader recited in Claim 1 wherein the input data types can include any one of a plurality of data modulation schemes.

56. The despreader recited in Claim 1 wherein the despreading code can include any one of a plurality of code modulation schemes.